



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,055	09/24/2001	Masaaki Hiroki	0756-2367	6718
31780	7590	06/03/2008		
ERIC ROBINSON			EXAMINER	
PMB 955			QI, ZHI QIANG	
21010 SOUTHBANK ST.			ART UNIT	PAPER NUMBER
POTOMAC FALLS, VA 20165			2871	
		MAIL DATE	DELIVERY MODE	
		06/03/2008	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 09/961,055	<b>Applicant(s)</b> HIROKI ET AL.
	<b>Examiner</b> Mike Qi	<b>Art Unit</b> 2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(o).

#### Status

1) Responsive to communication(s) filed on 23 April 2008.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 6,7,9,19,21,39,40,42,44-47 and 59-73 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 6,7,9,19,21,39,40,42,44-47 and 59-73 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. 07/837,394.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date 4/23/08

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_

5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_

**DETAILED ACTION**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 23, 2008 has been entered.

***Specification***

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6, 7, 9, 19, 21, 39, 40, 42, 44-47, 59-61 and 64-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,051,570 (Tsujikawa et al) in view of US 4,007,294 (Woods et al), US 4, 924,279 (Shimbo) and further in view of US 4,778,258 (Parks et al).

Regarding claims 6, 7, 9, 39, 40, 42, 59–61, 64 and 65, Tsujikawa teaches  
(col.10, line 36 - col.11, line 39; Fig. 9) an electro-optical display device (liquid crystal display device) comprising:

- a first substrate (128) having an insulating surface (glass substrate);
- at least one thin film transistor (103,104) formed over the first substrate (128), the thin film transistor (103,104) having a semiconductor film including channel region, source and drain regions, such as electrodes (117,118) with the channel forming region extending therebetween (the electrodes and the channel region should be formed in a semiconductor layer), and a gate electrode (112, 113) over gate insulating film (such as 134, 135), and because the dielectric film (121) also having a function as gate insulating film, so that such insulating film (121) having a source contact hole or a drain contact hole as a first and second contact holes at the left side and right side of the channel region as shown in Fig.9B;
- an interlayer insulating film (122) formed over the thin film transistor (103,104), and such interlayer insulating film (122) having a contact hole such as one of the source contact hole or the drain contact hole, so that the interlayer insulating film (122) would have a second contact hole ;
- an electrode (such as 118) formed over the interlayer insulating film (122) and electrically connected to the source region or drain region through contact holes (first and second or source and drain contact holes) of the interlayer insulating film (122), so that the electrode (such as 118) is in contact with the

one of the source and drain regions in the first contact hole (one of the contact holes);

- a leveling film (123) comprising organic resin formed over the electrode (such as 118), because the interlayer insulating film (123) formed of polyimide (organic resin) and functions as flatten the surface as shown in the Fig.9, and such leveling film (123) has a third contact hole as shown in Fig.9B;
- a pixel electrode (124) formed over the leveling film (123) and electrically connected to the electrode (such as 118) through the third contact hole as shown in Fig.9;
- such third contact hole is located apart from or does not overlap the first contact hole and the second contact hole (source contact hole and drain contact hole ) as shown in Fig.9B;

(concerning claims 9, 42, 59, 60, 64 and 65)

- silicon oxide film (141) functions as a blocking layer formed over the substrate (128), and the semiconductor film (channel forming region) is surrounded by the blocking layer (141) and the gate insulating film (134, 135, 121) as shown in Fig.9B;

(concerning claims 39, 40, 42 and 60)

- the electro-optical display having an active matrix type display can be used in any electronic device such as camera in the preamble of the claims that are only given weight as intended use, and that would have been at least obvious.

Tsujikawa further teaches that the gate insulating film is formed of silicon oxide

Art Unit: 2871

(see col.8, lines 16-18, that is the same as shown in the Fig.9 of the gate insulating film 134,135, and the dielectric film 121 also can be formed of silicon oxide as the insulating property and that is obvious in the art), but Tsujikawa does not explicitly teach that:

- 1) the gate insulating film contains fluorine;
- 2) the gate insulating film covering the semiconductor film and in contact with a top surface and side surfaces of the semiconductor film;
- 3) the pixel electrode is transparent.

**Woods** teaches (abstract) that a method of treating a layer of silicon dioxide in which an fluoride compound is applied to one surface of the silicon dioxide layer to prevent the deleterious effect resulting from any mobile impurity ions therein, so that would obtain more protection.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the electro-optical display device of Tsujikawa with the teachings of the gate insulating film having fluorine as taught by Woods, since the skilled in the art would be motivated for preventing the deleterious effect resulting from any mobile impurity ions therein (abstract).

Tsujikawa and Woods teach the invention set forth above except for that the gate insulating film covering the semiconductor film and in contact with a top surface and side surfaces of the semiconductor film, and the pixel electrode is transparent.

**Shimbo** teaches (col.2, lines 32-38; Figs.2-4) that the gate insulating film (6) covering the semiconductor film (5) and in contact with a top surface and side surface of the semiconductor film (5), and such TFT can be easily obtained.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the electro-optical display device of Tsujikawa and Woods with the teachings of the gate insulating film covering the semiconductor film as taught by Shimbo, since the skilled in the art would be motivated for easily obtaining a TFT.

Concerning pixel electrode is transparent that would be a conventional.

**Parks** teaches (col.5, lines 15-20) in general, pixel electrode having transparent material (transparent pixel electrode), and that is particularly useful in LCD displays in which back lighting is employed to form or assist in forming the desired image.

Therefore, it would have been obvious to those skilled in the art at time the invention was made to modify the electro-optical display device of Tsujikawa, the film treatment of Woods, and the gate insulating film covering the semiconductor film of Shimbo with the teachings of using transparent pixel electrode as taught by Parks, since the skilled in the art would be motivated for achieving a desired image, particularly, for the transmission type liquid crystal display as indicated in paragraph [0147] of this application.

Regarding claims 19, 44, 66 and 67, Tsujikawa teaches (col.11, lines 18-23; Fig.9) that the liquid crystal (125) is disposed between the first substrate (128) and the second substrate (127), and that is conventional.

Regarding claims 21, 45, 68 and 69, Tsujikawa teaches (col.11, lines 30-33; Fig.9) that the leveling film (123) comprises polyimide, because the interlayer insulating

film (123) functions as flatten the surface as shown in the Fig.9, such that the interlayer insulating film (123) is a leveling film.

Regarding claims 46, 70 and 71, Tsujikawa teaches (col.10, lines 43-55; Fig.9) that the channel region (between the source region and the drain region of the thin film transistor) comprises crystalline silicon.

Regarding claims 47, 72 and 73, Tsujikawa teaches (col.8, line 16-18) the gate insulating film comprises silicon oxide (the Fig.6 shows the same as the Fig.9 for the gate insulating film 134, 135, and the dielectric film 121 also can be formed of silicon oxide as the insulating property and that is obvious in the art).

5. Claims 62-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujikawa, Woods, Shimbo and Parks as applied to claims 6, 7, 9, 19, 21, 39, 40, 42, 44-47, 59-61, and 64-73 above, and further in view of US 5,054,887 (Kato et al).

Regarding claims 62-63, Tsujikawa, Woods, Shimbo and Parks teach the invention set forth above except for the gate electrode does not overlap the pixel electrode.

Kato teaches (see Fig.1 and 2) that the gate electrode (28) does not overlap the pixel electrode (24), and that is a common and known in the art as normal arrangement the pixel electrode does not overlap the TFT formed region, and that would have been at least obvious.

***Response to Arguments***

6. Applicant's arguments filed on April 23, 2008 have been fully considered but they are not persuasive.

In response to applicant's arguments that the prior art of references do not teach or suggest that a gate insulating film has a first contact hole, an electrode is in contact with one of the source and drain region in the first contact hole, and a third contact hole is located apart from or does not overlap the first contact hole and a second contact hole, It is respectfully pointed out that the reference Tsujikawa teaches that the dielectric film (121) also having a function as gate insulating film as the insulating property, so that such insulating film (121 and 134, 135 together) having a source contact hole and a drain contact hole as a first and second contact holes at the left side and right side of the channel region as shown in Fig.9B; and an electrode (such as 118 in Fig.9B) is in contact with one of the source and drain regions in a contact hole, and the leveling film (123) having leveling function also having a third contact hole is located apart or does not overlap with first contact hole and a second contact hole as shown in Fig.9B.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 7:30 am-6:00 pm.

Art Unit: 2871

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mike Qi/  
Primary Examiner, Art Unit 2871